Atty. Docket No. PIA31191/ANS/US
Serial No: 10/765,027

Remarks

Applicant and his representatives wish to thank Examiner Novacek for the very helpful and courteous discussion held with their undersigned representative on March 17, 2006. As suggested at the end of the discussion, Applicant has amended claim 1 to recite that removing part of the first nitride and first oxide layers and etching the substrate, including the lightly doped drain, by a depth of about 200 to about 1000 angstroms defines the gate region. Similarly, Applicant submits new claim 8, containing similar limitations (removing part of the first nitride layer and etching the exposed substrate, including the LDD, to a predetermined depth defines the gate region). The following remarks shall further summarize and expand upon topics discussed.

The present invention relates to a method for manufacturing a MOSFET device. In a first aspect, the method comprises:

a) forming a shallow trench isolation in a substrate;

b) forming a first oxide layer on a surface of an active region of the substrate and implanting ions thereinto for forming a lightly doped drain in the active region prior to the formation of a gate;

c) forming a first nitride layer;

d) removing a part of the first nitride layer and the first oxide layer and etching the substrate corresponding to the part, including the lightly doped drain, by a depth of about 200 to about 1000 angstroms to define a gate region;

e) forming a second oxide layer over an exposed portion of the substrate;

f) implanting ions into the substrate;

g) removing the second oxide layer;

h) depositing a gate insulating layer and a polysilicon layer into the removed parts of the first nitride layer and the first oxide layer;

i) polishing until the first nitride layer is exposed;

j) removing the first nitride layer, depositing an oxide layer conformally and depositing a second nitride layer;

k) etching the second nitride layer to form a gate sidewall;

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l) implanting ions into the substrate to form a source and drain at sides of the gate; and

m) removing an exposed oxide layer (see amended Claim 1 above).

In a second aspect, the method comprises:

1) implanting ions into an active region of a substrate to form a lightly doped drain (LDD) prior to forming a gate;

2) forming a first nitride layer on the substrate, including the active region;

3) removing part of the first nitride layer and etching the exposed substrate, including the LDD, to a predetermined depth to define a gate region;

4) implanting ions into the substrate to control a voltage threshold of the MOSFET device;

5) forming a gate insulating layer and a polysilicon layer in the gate region;

6) removing the first nitride layer, then depositing an oxide layer and a second nitride layer on the polysilicon layer;

7) etching the second nitride layer to form a gate sidewall; and

8) implanting ions into the substrate to form a source and drain at sides of the gate (see new Claim 8 above).

The references cited against the present application (Li et al., U.S. Pat. No. 6,309,933 [hereinafter "Li et al."], Yagashita et al., U.S. Pat. No. 6,607,952 [hereinafter "Yagashita et al."], Lee et al., U.S. Pat. No. 5,583,064 [hereinafter "Lee et al."], and Bovaird, U.S. Pat. No. 4,830,975 [hereinafter "Bovaird"]) neither disclose nor suggest removing part of a nitride layer and etching the exposed substrate, including the LDD, to a depth to define a gate region, forming a gate insulating layer and a polysilicon layer in the gate region (i.e., the removed part of the nitride layer), removing the first nitride layer, then depositing an oxide layer and a second nitride layer on the polysilicon layer, and etching the second nitride layer to form a gate sidewall (see

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amended Claim 1 and new Claim 8 above). Consequently, the present claims are patentable over the cited references.

The Rejection of Claims 1-4 and 6-7 under 35 U.S.C. § 103(a)

The rejection of Claims 1-4 and 6-7 under 35 U.S.C. § 103(a) as being unpatentable over Li et al. in view of Yagashita et al. and Lee et al. is respectfully traversed.

Li et al. discloses a method of fabricating a semiconductor transistor device in which a semiconductor structure is provided having an upper silicon layer, a pad dielectric layer over the upper silicon layer, and a well implant within a well region in the upper silicon layer (Abstract, ll. 1-5). A lower SiN layer is deposited and patterned over the pad dielectric layer to define a lower gate area, then the pad dielectric layer and the upper silicon layer within the lower gate area are etched to form a lower gate trench having a predetermined width (Abstract, ll. 5-9). A lower gate portion is formed within the lower gate trench, then an upper oxide layer is formed over the lower SiN layer and an upper SiN layer is formed over the upper oxide layer (Abstract, ll. 9-12). The upper SiN layer is etched to define an upper gate trench having a predetermined width greater than the lower gate trench (Abstract, ll. 12-15). An upper gate portion is formed within the upper gate trench, wherein the lower and upper gate portions form a T-shaped gate (Abstract, ll. 15-17). The etched upper SiN, upper oxide, and lower SiN layers are removed to expose the T-shaped gate extending above the pad dielectric layer (Abstract, ll. 17-19). An uppermost oxide layer is formed over the exposed T-shaped gate, and SiN sidewall spacers are formed adjacent the exposed vertical side walls of the lower polysilicon gate portion (Abstract, ll. 19-22).

However, as shown in FIGS. 12-14 of Li et al., after forming uppermost oxide layer 62 over upper poly gate portion 58 and lower poly gate portion 44, and after depositing uppermost SiN film 64 over pad oxide/dielectric layer 12 and uppermost oxide layer 62, then removing the same by a dry anisotropic etch, stopping on pad oxide/dielectric layer 12 and uppermost oxide layer 62, LDD (low doped source/drains) implants 65 are formed (e.g., by an angled LDD ion

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implantation) in the substrate 10 (also see col. 5, ll. 30-57 of Li et al.). Thus, Li et al. neither disclose nor suggest removing part of a nitride layer and etching the exposed substrate, ***including the LDD***, to a particular depth to define a gate region.

Neither Yagashita et al. nor Lee et al. cure the deficiencies of Li et al. with regard to the present claims.

Yagashita et al. disclose a method of manufacturing a semiconductor device that includes the steps of forming a disposable gate on a semiconductor substrate in a region where a gate electrode is to be formed, forming a sidewall spacer on a sidewall of the disposable gate, forming a source and drain in the semiconductor substrate using the disposable gate and the sidewall spacer as a mask, forming an interlevel insulating film on the semiconductor substrate so as to cover the disposable gate, planarizing an upper surface of the interlevel insulating film to expose upper surfaces of the disposable gate and the sidewall spacer, removing the disposable gate to form a trench portion having a side surface formed from the sidewall spacer and a bottom surface formed from the semiconductor substrate, depositing a gate insulating film on the semiconductor substrate so as to cover the bottom surface and side surface of the trench portion, forming a gate electrode buried in the trench portion, and removing the sidewall spacer and the gate insulating film on the sidewall of the gate electrode (Abstract). Similar to Li et al., Yagashita et al. implant ions using a disposable gate 33 as a mask to form a n$^+$-type source and drain 16 (col. 5, ll. 52-54 and FIG. 2E of Yagashita et al.).

Thus, Yagashita et al. cannot disclose or suggest removing part of a nitride layer and etching the exposed substrate, ***including the LDD***, to a particular depth to define a gate region, as is recited in amended Claim 1 and new Claim 8. Therefore, Yagashita et al. does nor cure the deficiencies of Li et al. with regard to the present claims.

Lee et al. disclose forming a recess into the surface of a substrate to form a gate channel in the recess, so that a monocrystalline source/drain region can be formed at a level higher than that of the channel (Abstract, ll. 1-4). The process includes the steps of: (a) forming an insulating layer and an oxidation preventing layer on a semiconductor substrate, and removing

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the oxidation preventing layer of a channel region of the transistor by an etching process; (b) forming an oxide layer on the channel region of the transistor by thermally oxidizing the semiconductor substrate, removing the oxidation preventing layer, and carrying out a first ion implantation on the whole surface; (c) removing the oxide layer, and forming the channel of the transistor in the form of a recess so as for the recess to be positioned lower than the surface of the substrate; (d) forming a gate electrode in the recess; and (e) carrying out a second ion implantation on the whole surface, and carrying out a heat treatment to form a source/drain region (Abstract of Lee et al., ll. 4-18).

In both embodiments of Lee et al. depicted in the Figures, the ion implantation to form a LDD is carried out after formation of a mask structure in the region where the gate is formed. For example, an oxidation process for forming a transistor channel region is carried out at a temperature of about 900 °C. such that the thickness of oxide layer 55 becomes about 2500 Å (see col. 5, ll. 22-26 and FIG. 5C of Lee et al.). Thereafter, nitride layer 53 is removed, and a first ion implantation is carried out. At the next step, the ion implanted impurity is diffused by applied heat, thereby forming LDD region 56 (see col. 5, ll. 27-34 and FIGS. 5D-5E of Lee et al.). Then, the thick oxide layer 55 for forming the channel is removed by dipping into an aqueous HF solution (50:1), and thus the channel region is made to have an elliptical cross section (see col. 5, ll. 35-38 and FIG. 5E of Lee et al.). Thereafter, gate insulating layer 57 is formed by an oxidation process at a temperature of about 850 °C., thereby forming an SiO_2 layer with a thickness of about 100 Å, then doped polysilicon layer 58 containing phosphorus ions is deposited in-situ, and silicon oxide layer 59 is deposited to a thickness of about 1500 Å (see col. 5, ll. 38-45 and FIG. 5E of Lee et al.). Then, gate line 58' is defined by applying a photolithography (see col. 5, ll. 46-47 and FIG. 5F of Lee et al.). Thus, the embodiment of FIGS. 5A-5H of Lee et al. do not disclose or suggest a process that removes part of a nitride layer and etching the exposed substrate, ***including the LDD***, to a particular depth to define a gate region, as recited in amended claim 1 and new claim 8.

Alternatively, in a second embodiment, Lee et al. define the gate line of the transistor by photolithography and RIE-etching Si_3N_4 layer 63 (col. 6, ll. 25-28 and FIG. 6B). However, the

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portion of the silicon substrate which is not protected by nitride layer 63 is thermally oxidized to form SiO_2 layer 65 (col. 6, ll. 29-34 and FIG. 6C of Lee et al.). Then, as illustrated in FIG. 6D, silicon oxide layer 65 is etched using nitride layer 63 as a mask ***until silicon substrate 61 is exposed*** (col. 6, ll. 35-37 of Lee et al.; emphasis added). A gate insulating layer 66 is then formed by thermal oxidation (col. 6, ll. 38-41 and FIG. 6D of Lee et al.). Polysilicon layer 67 is deposited to a thickness of about 3500 Å to completely fill the recess over the transistor gate channel (col. 6, ll. 42-48 and FIG. 6E of Lee et al.), then the polysilicon layer is etched until silicon nitride layer 63 becomes exposed, so that gate line 68 may automatically be formed in a recessed shape (col. 6, ll. 49-52 and FIG. 6F of Lee et al.). Thereafter, Si_3N_4 film 63 is removed, and a high concentration As^+ ion implantation is carried out to form an n^+ source/drain region. Then, as illustrated in FIG. 6H, SiO_2 layers 62 and 65 are removed, and an n^- source/drain region (LDD) is formed by low concentration ion implantation (col. 6, ll. 53-65 and FIGS. 6G-6H of Lee et al.). Thus, the embodiment of FIGS. 6A-6I of Lee et al. do not disclose or suggest a process that removes part of a nitride layer and etching the exposed substrate, ***including the LDD***, to a particular depth to define a gate region, as recited in amended claim 1 and new claim 8.

As a result, Lee et al. fails to cure the salient deficiencies of Li et al. and Yagashita et al. with regard to the present claims. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 5 under 35 U.S.C. § 103(a)

The rejection of Claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Li et al. in view of Yagashita et al., Lee et al. and Bovaird is respectfully traversed.

As explained above, the combination of Li et al., Yagashita et al., and Lee et al. fails to disclose a method that includes removing part of a nitride layer and etching the exposed substrate, ***including the LDD***, to a particular depth to define a gate region, as recited in amended claim 1 and new claim 8. One of ordinary skill in the art would not look to Bovaird to cure this

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deficiency, as Bovaird does not provide motivation to combine a method that includes removing part of a nitride layer and etching the exposed substrate, ***including the LDD***, to a particular depth to define a gate region with a method that forms a gate in a recess, then forms a sidewall spacer from a nitride layer deposited on the gate.

Bovaird discloses a PRIMOS (Planar Recessed Isolated MOS) transistor and a method for fabricating same, wherein the source and drain in a semiconductor body are separated by a recess. A gate oxide is disposed on the body in the recess, with conductive gate material thereon. Oxide regions are positioned on each side of the gate, ***such oxide regions being substantially thicker in cross-section than the gate oxide*** (Abstract of Bovaird, ll. 1-8; emphasis added). By forming oxide regions on each side of the gate that are substantially thicker in cross-section than the gate oxide, Bovaird avoids any need to form a sidewall spacer from a nitride layer deposited on the gate. As a result, Bovaird is silent with regard to depositing any material on the gate (see, e.g., col. 3, ll. 10-30; col. 3, l. 61-col. 4, l. 17; and col. 4, l. 63-col. 5, l. 17 of Bovaird), much less forming a sidewall spacer out of it.

It is well-established that, before a conclusion of obviousness may be made based on a combination of references, there must have been a reason, suggestion or motivation to lead an inventor to combine those references. *Pro-Mold and Tool Co. v. Great Lakes Plastics*, 75 F.3d 1568, 37 USPQ2d 1626 (Fed. Cir. 1996). The reason, suggestion or motivation cannot come from the Applicant's invention itself. *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). By its silence with regard to depositing a material on the gate and by its repeated teaching of techniques that avoid any need or desirability of a sidewall spacer formed from a material deposited on a gate, Bovaird cannot be properly combined with Li et al., Yagashita et al., and Lee et al. to reject the present claims for obviousness.

As a result, this ground of rejection is unsustainable, and should be withdrawn.

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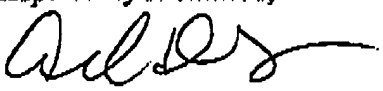
Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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